Remarks

In view of the above amendments and the following remarks, reconsideration and further examination are requested.

Claims 1-4 have been rejected under 35 U.S.C. §102(e) as being anticipated by Cho (US 6,158,039). Claim 1 has been amended so as to further distinguish the present invention from this reference. Further, claim 4 has been canceled without prejudice or disclaimer to the subject matter contained therein.

The above-mentioned rejection is submitted to be inapplicable to the claims for the following reasons.

Claim 1 is patentable over Cho, since claim 1 recites a signal processor including, in part, an error correction block operable to subject data, which has been stored in a first memory, to error correction for each predetermined error correction block; a second memory; a descrambling/error detection block operable to read the data after the error correction from the first memory, descramble the data which has been subjected to the error correction, detect errors in the data after the descrambling, and thereafter store the data in the second memory; and a controller operable to transmit error-free data which has been stored in the second memory to a host computer when the descrambling/error detection block judges that there is no error in the data which has been stored in the second memory, wherein, when the descrambling/error detection block judges that there is an error in the data stored in the second memory, the data stored in the second memory are read out for each predetermined error correction block, and subjected to error correction by the error correction block. Cho fails to disclose or suggest a second memory as is now recited in claim 1.

Cho discloses a system decoder 18 having an ECC memory controller 108, a third memory 130, a fourth memory 140, an error corrector 110, a descrambler and error detector 112, a buffer write controller 114, a microprocessor memory access controller 116, a buffer read controller 118, and a second memory 30. The ECC memory controller 108 receives demodulated data from an EMF demodulator 100. The system decoder 18 operates such that the controller 108 writes one correcting block of the received demodulated data into the third memory 130 in a first step. In the next step, the error corrector 110 error-corrects the data written in the third memory 130 and the controller 108 writes the next one correcting block of the received demodulated data into the fourth memory 140.

In the next step, the error corrector 110 error-corrects the data written in the fourth memory 140, and the controller 108 simultaneously outputs the error-corrected data from the third memory 130 to the descrambler and error detector 112 and inputs the next one correcting block of the received demodulated data to the third memory 130. In the next step, the error corrector 110 error-corrects the data written in the third memory 130, and the controller 108 simultaneously outputs the error-corrected data from the fourth memory 140 to the descrambler and error detector 112 and inputs the next one correcting block of the demodulated data to the fourth memory 140. The above process is repeated until the demodulated data is no longer receives from the EMF demodulator 100.

The descrambler and error detector 112 alternatively receives the error-corrected data from the third memory 130 and the fourth memory 140 and restores the data scrambled during an encoding process and detects any errors in the descrambled data. The buffer write controller 114 under control of the microprocessor memory controller 116 then stores the descrambled data and any error information in the second memory 30. Next, the buffer read controller 118 also under control of the microprocessor memory controller 116 reads the data stored in the second memory 30 and transmits the data to an A/V decoder interface and a DVD-ROM interface 126. (See column 2, lines 38-60; column 3, lines 34-43; column 4, line 38 - column 5, line 21; and Figures 2-4).

Based on the above discussion, there are three memories that are utilized in the system decoder 18 of Cho. These memories are the second memory 30, the third memory 130 and the fourth memory 140. However, none of the memories of Cho corresponds to the second memory recited in claim 1.

The third memory 130 and the fourth memory 140 are operable to alternatively receive correcting blocks from the controller 108 and once the correcting blocks are error corrected by the error corrector 110, the error-corrected data is alternatively output from the third memory 130 and the fourth memory 140 to the descrambler and error detector 112 to make room for the following correcting blocks. In other words, the correcting blocks in the third memory 130 and the fourth memory 140 are always error corrected by the error corrector 110 and then sent to the descrambler and error detector 112 . On the other hand, the present invention as claimed in claim 1 recites a second memory that has data stored therein after the data passes through a descrambling/error detection block which reads the data after error correction from a first memory, descrambles the data

which has been subject to the error correction, and thereafter stores the data in the second memory, wherein when the data stored in the second memory are judged by the descrambling/error detection block as having no errors, the data stored in the second memory are transmitted to a host computer and when the data stored in the second memory are judged to contain an error, the data stored in the second memory are read out for each predetermined error correction block and subjected to error correction. It is apparent that, in Cho, there is no judgment as to whether or not the correcting blocks stored in the third memory 130 and the fourth memory 140 have errors before sending the correcting blocks to the error corrector 110. Instead, the correcting blocks are always sent to the error corrector 110 before being transmitted to the descrambler and error detector 112. Therefore, neither the third memory 130, nor the fourth memory 140, corresponds to the second memory recited in claim 1.

The second memory 30 of Cho receives descramble data and any error information detected by the descrambler and error detector 112 and stores the descramble data and the error information. The data in the second memory 30 is read out and transmitted to the A/V decoder interface and the DVD-ROM interface 126. In other words, even though the descrambler and error detector 112 might detect an error in the descramble data and this error information is stored in the second memory 30, no error correction is performed on the descramble data. Instead, the data in the second memory 30 is transmitted to the A/V decoder interface and the DVD-ROM interface 126 regardless of whether or not an error has been detected. Therefore, the second memory 30 also fails to correspond to the second memory recited in claim 1.

As a result, it is apparent that Cho fails to disclose or suggest the present invention as recited in claim1.

Because of the above-mentioned distinctions, it is believed clear that claims 1-3 are not anticipated by Cho. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to modify Cho or to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1-3. Therefore, it is submitted that claims 1-3 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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